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TEXAS INSTRUMENTS INCORPORATED			MICHELL, JAMES M	
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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/164,580
Filing Date: October 01, 1998
Appellant(s): ARNOLD ET AL.

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GROUP 2800

Jay Cantor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 13, 2004.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is substantially correct. The changes are as follow to applicant's second issue: claims 22-31 involve two distinct issues of:

- 1) an appealable matter of whether claims 22-31 are anticipated by Potter (U.S. 6,028,437);

2) and whether an interference should have been provoked pursuant to 37 C.F.R. 1.608, which relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 120.

The appealable matters are addressed in this examiner's answer.

(7) *Grouping of Claims*

The brief includes a statement that claims do not stand or fall together, but fails to present reasons in support thereof as required under 37 CFR 1.192(c)(7). MPEP § 1206.

(8) *ClaimsAppealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

U.S. 6,005,778	Spielber et al.	December 21, 1999
U.S. 5,633,535	Chao et al.	May 27, 1997
U.S. 6,728,113	Knight et al.	April 27, 2004
U.S. 6,028,437	Potter et al.	February 22, 2000

(10) *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims as set forth in a prior Office Action, mailed on August 5, 2004.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9, 10, 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Knight et al. (U.S. 6,728,113).

Knight discloses (Fig 5) discloses (cl. 9) an interconnecting layer for use in a semiconductor package which comprises, (a) an electrically insulating layer (70; "ceramic"; Col. 20, Lines 8-14), (b) electrically conductive paths (76-78) on said layer, each of said paths having first (Left portion i.e. 77) and second (Right portion) spaced apart (i.e. middle portion) regions thereon, said second spaced apart region of each of said paths having a compliant bump ("conductive connections...fabricated by ...compliant...contacts;" not labeled; Col. 20, Lines 22-28) having a height greater than all other structures on said layer; and (c) a standoff ("spacers"; not shown; Col. 16, Lines 59-60) disposed on said layer (i.e. in a position above layer) and having a height above said layer and less than said bump (i.e., bump also penetrates item 10); (cl. 10) wherein the layer said second region is a bump extending above the level of said electrically conductive path (i.e. compliant bump); (cl. 13 and 14) and said interconnection layer is flexible (Col 20, Lines 8-14).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 22-31 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Potter (U.S 6, 028, 437).

(11) Response to Argument

Issue 1

Knight et al. (U.S. 6,728,113) anticipates the claims, because the claim language is disclosed by the prior art.

Applicant contends that Knight does not disclose an “electrically insulating layer, electrically conductive paths on the layer, each path having first and second spaced apart regions thereon, the second spaced apart region having a compliant bump greater than all other structures on the layer,” because: 1) the conductive connections are not numbered; 2) it is not clear what they [connective connections] are from the specification and drawings; 3) there is no basis to ascribe the structure and function to these unnumbered elements; 4) there is no basis for spacers corresponding to standoffs ; 5) standoff disposed on a layer having a height less than the bump; or 6) there is no correlation between what examiner alleges is the standoff and bump.

The specification and drawing define the function and structure of the unnumbered elements

Although it is true that the conductive connections shown in Figure 5 of Knight (U.S. 6,728,113) are not numbered, the specification in its description of Figure 5, defines the conductive region explicitly in Column 2, Lines 23-29, by indicating in part

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that "conductive connection between terminals 71, 72, 73...and similar on chip can be fabricated by compliant contact." The contact is disclosed in Figure 5 as a protuberance of material or bump that extends higher than all the other structures between the chip, 11, and substrate, 10, of Knight. Because Knight provides an exact pin-point location of its conductive connection between terminals on the chip and substrate, which is clear and unambiguous, wherein the exact placement of the connections are not subject to multiple interpretations, Knight's disclosure provides a basis for defining the conductive connection's structure (i.e. bump) and function (i.e. compliant). Since Knight provides the basis to ascribe the structure and function of the unnumbered elements, for the reasons *supra*, applicant's claims are not patentable over Knight.

A spacer is a standoff

Applicant has argued through mere conjecture that there is no basis for spacers being standoffs, but has provided no evidence to buttress his position. These arguments alone cannot take the place of evidence in the record. See *In re Budnick*, 537 F.2d at 538, 190 USPQ at 424; *In re Schulze*, 346 F.2d 600, 145 USPQ 716 (CCPA 1965); *In re Cole*, 326 F.2d 769, 140 USPQ 230 (CCPA 1964).

Knight explicitly discloses spacers, which function to provide separation between materials, as indicated in Knight (Col. 16, Lines 59-60). The term spacers and/ or standoffs are used in the art interchangeably in reference to a structure capable of providing separation between materials. Evidence of the terms interchangeability is found in Spielberger et al (U.S 6,005,778) at column 2, lines 22-26 and Chao et al (U.S.

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5,633,535) in its abstract. Because Knight explicitly discloses a spacer, there is basis for examiner referring to them as standoffs.

The spacer physically must be placed in an area smaller than the conductive bumps to assure separation of half capacitor plates

Applicant argues generally that there is no correlation between what examiner alleges is the bumps and the standoff in Knight, and that there is no basis for the allegation, without further scrutinizing the elements cited by examiner or providing actual evidence that examiner's rejection was improper. Note that applicant's argument cannot rebut a *prima facie* case. See M.P.E.P section 2145 [R-2], which says in part:

The arguments of counsel cannot take the place of evidence in the record. In re Schulze, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965); In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997) ("An assertion of what seems to follow from common experience is just attorney argument and not the kind of factual evidence that is required to rebut a *prima facie* case of obviousness.")

Because applicant did not provide an adequate rebuttal, examiner's rejection should be maintained.

Examiner agrees that the correlation between the spacers/standoff¹ and the compliant bump is not shown in Figure 5, but that the spacer placement can be reasonably determined by Knight's written description.

Knight discloses spacers (i.e. "on the chip"; Col. 16, Lines 59) in close proximity to intermediate substrate, 10, and in the presence of dielectric material, 17, which assures separation (i.e. capacitor plates 14, 15; Fig. 4, 5); the concern of capacitor

¹ The term spacer and standoff are interchangeable as shown, *supra*.

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plates and its performance is a concern of Figure 5. The separation is important between the plates, because Knight discloses that changes in separation, can result in shorting/cross talk (Col. 16, Lines 60-61; Col. 17, Lines 30-34) depending on the type of dielectric material between the plates, which affects the performance of the capacitors (Column 16, Lines 19-20). Because one of ordinary skill in the art would be reasonably apprised that the spacer would have to placed in the opening defined by the chip, 11 and an intermediate substrate, 10, as shown in Figure 5, such that it height is larger than conductive paths (i.e. 52), but less than that of the compliant bumps in order to assure the appropriate separation between layers (14, 15), examiner's rejection should be maintained. Contrary to applicant's arguments, there is a basis for examiner's allegations as shown in Knight as indicated, *supra*.

Issue 2

Potter anticipates the claimed invention, because the claims were copied from Potter (U.S 6,028,437). Although applicant contends that Potter rejection is without merit, he fails to explain why examiner's rejection and argument was improper.

Claims were copied from Potter and therefore claims the same patentable invention
37CFR 1.131 says in part:

Prior invention may not be established under this section if either:

- (1) The rejection is based upon a U.S. patent or U.S. patent application publication of a pending or patented application to another or others which **claims the same patentable invention** as defined in § 1.601(n) [emphasis mine]

37 C.F.R 1.601(n) says in part:

(n) Invention "A" is the same patentable invention as an invention "B" when invention "A" is the same as (35 U.S.C. 102)

Applicant's statement that, "the declaration establishes a date of invention prior to... Potter," is contrary to the express language of 37 C.F.R 1.131, since examiner rejection is based on 35 U.S.C 102, as evidenced by the claim language and applicant's admission to copying Potter [Page 5 of Brief]. Furthermore, applicant has neither cited a primary or secondary source that creates an exception to the statute, which would effectuate applicant's claim of prior invention. Per 37 CFR 1.131, a declaration cannot be used to swear behind a reference claiming the same subject matter, as such, examiner's rejection pursuant to 35 U.S.C 102 should be maintained.

Respectfully submitted,


James Mitchell
April 4, 2005

Conferees

James Mitchell

Carl Whitehead Jr.

Brian Sircus



TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265